CLAIMS

We claim:

1. ~~A bridge~~ comprising:

a plurality of interface registers that are configured to facilitate communication of data with a plurality of function units, and

a plurality of register transfer units, operably coupled to the plurality of interface registers, that facilitate transfers of data among interface registers of the plurality of interface registers.

2. The bridge of claim 1, further including

an instruction memory that is configured to contain register transfer instructions, wherein

the operable coupling of the plurality of register transfer units and the plurality of function units is effected via the register transfer instructions.

3. The bridge of claim 1, further including:

at least one datapath unit, operably coupled to the plurality of register transfer units, that facilitate a transformation of at least one data item of the data that is transferred among the interface registers.

4. The bridge of claim 3, further including

an instruction memory that is configured to contain register transfer instructions, wherein

the operable coupling of the plurality of register transfer units and the plurality of function units and the at least one datapath unit is effected via the register transfer instructions.

5. The bridge of claim 1, wherein

at least one of the function units is a programmable digital signal processor.

6. A signal processing system comprising:

a receiver that is configured to provide a digital input stream,

a channel decoder, operably coupled to the receiver, that is configured to decode the digital input stream into a decoded signal stream, and

a user application, operably coupled to the channel decoder, that is configured to render an output corresponding to a channel of the digital input stream based on the decoded signal stream,

wherein

the channel decoder comprises

a bridge comprising:

a plurality of interface registers, each associated with a processing unit of a plurality of processing units,

a plurality of register transfer units, operably coupled to the plurality of interface registers, that facilitate:

transfers of data among interface registers of the plurality of interface registers,

transfers of data of the digital input stream among interface registers of the plurality of interface registers, and

transfers of data from the interface registers to provide the decoded signal stream.

7. The signal processing system of claim 6, wherein

the channel decoder further includes

an instruction memory that is configured to contain register transfer instructions,

wherein

the operable coupling of the plurality of register transfer units and the plurality of processing units is effected via the register transfer instructions.

8. The signal processing ~~system of claim 6, further including~~g:

at least one datapath unit, operably coupled to the plurality of register transfer units, that facilitate a transformation of at least one data item of the data that is transferred among the interface registers.

9. The signal processing system of claim 8, wherein

the channel decoder further includes

an instruction memory that is configured to contain register transfer instructions, wherein

the operable coupling of the plurality of register transfer units and the plurality of processing units and the at least one datapath unit is effected via the register transfer instructions.

10. The signal processing system of claim 6, wherein

at least one of the processing units is a programmable digital signal processor.

add C1

Add E1